What is claimed is:

1. A method of performing a design rule check on an integrated circuit, comprising:

tagging at least one line in a schematic with a width marker and an associated width parameter;

extracting the line width marker and the associated line width parameter;

comparing the extracted line width parameter with an actual design width for a design line; and

generating an error condition when the actual design line width is less than the line width parameter.

2. The method of claim 1, wherein comparing excludes areas on or above a transistor.

3. The method of claim 1, and further comprising indicating or recording the error condition.

4. The method of claim 1, wherein the line width parameter represents the minimum width for the design line.

5. The method of claim 1, wherein the actual design width for the design line is greater than a minimum width for the design line.

6. A method of performing a design rule check on an integrated circuit, comprising:

tagging at least one line with a width marker in a schematic;

extracting each line having a width marker in a layout;

extracting a width for each extracted line;

comparing the schematic versus the layout;

checking a layout line with the extracted width; and

generating an error condition for any line with a layout width less than its extracted width.

7. The method of claim 6, wherein comparing excludes areas on or above a transistor.

8. The method of claim 6, and further comprising indicating or recording the error condition.

9. The method of claim 6, wherein each line having a width marker has a width greater than a minimum width for that line.

10. The method of claim 6, wherein the extracted width for any line represents a minimum line width for that line.

11. A method of performing a layout versus schematic check on an integrated circuit, comprising:

comparing layout line widths with existing line width marker parameters for selected lines of the circuit; and

indicating an error if a layout line width is less than its line width marker parameter.

12. The method of claim 11, wherein the layout line widths are greater than an absolute minimum line width.

13. The method of claim 11, wherein the selected lines of the circuit carry power for transistors of the integrated circuit.

14. The method of claim 11, and further comprising extracting the line width parameters from the schematic and extracting the layout line widths from the layout before comparing.

15. The method of claim 11, and further comprising identifying the ends and measuring the widths of the selected lines of the circuit before comparing.